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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: Thomas Novet et al.	)	
	)	Attorney
Serial No: 10/626,171	)	Docket Number: 200210020-1
	)	
Filed: July 23, 2003	)	Group Art Unit: 2815
	)	
Title: Electron Emitter With Epitaxial Layers	)	Examiner: N. Drew Richards
	)	

DECLARATION OF INVENTORS UNDER
37 C.F.R. § 1.131

Thomas E. Novet, Paul J. Benning, Alexander Govyadinov and Robert Bicknell-Tassius make the following declaration.

1. We are the inventors of the subject matter claimed in the above captioned patent application. At the time of our invention, we were under an obligation to and did assign the invention to Hewlett-Packard Company (HP).

2. The claimed subject matter was conceived before April 17, 2003 as documented in the Invention Disclosure No. 200210020-1. A copy of the Invention Disclosure is attached to this Declaration as Exhibit A.

3. The Invention Disclosure was assigned to outside patent counsel Steve Fallon and Tom Fitzsimons at the firm of Greer, Burns and Cain to prepare the patent application. On April 16, 2003, the inventor approved draft patent application was submitted to Tim Myers, the HP in-house lawyer handling the case. Mr. Myers communicated his comments on the draft to Mr. Fitzsimons, and on May 7, 2003 Mr. Fitzsimons emailed us a revised/second draft patent application

incorporating Mr. Myers' comments. We approved the revised/second draft patent application on May 14, 2003. Copies of the April 16, May 7, and May 14 correspondence are attached to this Declaration as Exhibits B, C and D respectively.

4. Mr. Fitzsimons submitted the revised/second draft patent application to Mr. Myers on May 22 and Mr. Myers approved the draft for filing on June 10, 2003. On June 20, 2003, the finalized patent application and the signature papers prepared by Mr. Fitzsimons's office were sent to HP for signing and filing. The application was filed on July 23, 2003. Copies of the May 22 and June 10 and 20 correspondence are attached to this Declaration as Exhibits E, F and G respectively.

5. All of the activities related to this invention took place in the United States.

We declare that all statements made in this Declaration of our own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the patent application or any patent issued on that application.

8 December 2005
Date

Thomas E. Novet

Dec 8 2005
Date

Paul J. Benning

8 December 2005
Date

Alexander Govyadinov

Dec. 8, 2005
Date

Robert Bicknell-Tassius

Disclosure No. 200210020

Invention Disclosure - QBI Document No. SOJ

invent

PD No. 200210020

[redacted]

General Information

Title A Flat Electron Emitter with Epitaxial Layers

Abstract A high efficiency flat electron emitter is built with epitaxial distributed ballast resistor, dielectric, and conducting layers. This emitter delivers a steady, near collimated electron beam.

Projects [redacted]

Products

Attachments

Attachments Epitaxfet_1_.ppt - 10/9/02 4:58PM - Prior art and Innovation description (Uploaded by Alexander Govyadinov)

Inventor Information

Inventors			
Thomas E Noyur	Hewlett-Packard Company	Corvallis	[redacted]
Paul J Benning	Hewlett-Packard Company	Corvallis	
Alexander Govyadinov	Hewlett-Packard Company	Corvallis	
Robert Bicknell Tasalles	Hewlett-Packard Company	Corvallis	

EXHIBIT A
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United States [US]

Description of Invention

Problems Solved In order to concentrate an electron beam to a small spot, either the source must be small or the beam must be well collimated as it exits the emitter. Flat emitters give off electrons over a relatively large area thus electrons emitted from these emitters must have a minimum of angular divergence to be focusable.

Sources of beam divergence from traditional flat emitters includes both electric field non-uniformities arising from nonplanarity in the emitter surface and electron scattering within layers that comprise the emitter. Electrons that travel through thick layers of materials are far more likely to scatter off atoms or other electrons in the layer. Bumps or other geometrical imperfections in the stack will produce electrical fields that will accelerate electrons non-normal to the face of the emitter.

Epitaxial films can be grown very thin and extremely flat. They can be produced with atomically smooth surfaces and interfaces which exhibit no geometrical features that can lead to divergence. Since they are single crystal films, they are free from pinholes or other defects that can facilitate electrical breakdown. The crystalline nature of these films can also minimize electron scattering due to material nonuniformities. Very thin films, less than 20 nm thick, are sufficient for robust operation.

Prior Solutions Field emitters such as Spindt tips (J. Appl. Phys. 39, 3504 (1968)) and etched silicon tips (reference here) offer high emission currents at reasonable drive voltages. The current from these tips is unstable both temporally and spatially, varying from fifty to three hundred percent of the average value. Current and turn on energy is surface dependent, therefore dependent on surface contaminants and changes in tip geometry. Since tips are so dependent on shape and surface contaminants, it is difficult to manufacture a large number of emitters that have identical performance.

MIS flat (Pioneer patent, other papers) are much easier to manufacture, however they suffer from short lifetimes, low brightness, and poor efficiency. Without ballast resistors, they are subject to electrical damage through weak spots in the dielectric layer. Electrical scattering in the often thick dielectric layers leads to low efficiency and current density.

Porous Silicon Emitter (United States Patent 6,285,118; J of Vacuum Sci. and Technology B 19, PART 1 (2001) 85-87) US 6,285,118) and Poly Silicon Emitters (FEMIS - HPL patent application and CV flats - HP Patent Application No. 10019110) are in attempt to marry the best of tips and flats. Buried silicon tips in a dielectric layer offer higher current densities and efficiencies than traditional flat emitters, but high divergence, low brightness and low emission uniformity are an issue and the emitters have short lifetimes as large currents pass through.

Description The emitter is built as outlined in the attached file. An epitaxial semiconductor layer such as intrinsic silicon is deposited on n+ doped silicon. This semiconductor layer acts as a distributed ballast resistor, creates uniform emission from surface, and protects the device from run away electrical breakdown of the dielectric layer.

Next a thin, less than 20 nm thick, epitaxial dielectric film is deposited on the semiconductor layer. Aluminum nitride, silicon oxide, aluminum oxide, tantalum oxide, titanium oxide, hafnium oxide, or zirconium oxide, or superlattices of the above materials are examples of materials that can be used for this dielectric layer. These films can be deposited using atomic layer deposition. The film must be thick enough to hold off between 10 and 15 volts yet as thin as possible in order to minimize internal electron scattering.

Finally, an upper electrode is deposited on the emitter. This electrode can be a thin,

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less than 7 nm, metal layer such as gold or platinum or it can be an n-doped semiconductor such as phosphorus-doped silicon. This layer should also be as thin as possible to minimize internal scattering.

The device is operated by applying a potential between substrate and upper electrode. Electrons tunnel through dielectric and thin conductor into vacuum following a Fowler-Nordheim mechanism.

Advantages Flat emitters are much easier to build than tip emitters. A small difference in the geometry of a tip has a large effect on its emission. Spindt-tip emitter manufacture requires an evaporator with a collimated beam. Tip-to-tip variability is considerable.

The advantages of our flat over traditional flat emitter includes:
1. Distributed ballast resistor- reduce run away electrical breakdown and create truly uniform emission.
2. Epitaxial layer is very smooth and defectless, that lowers divergence. Thinner layers might be used, therefore emitter has higher emission current and higher efficiency.
3. ALD gives opportunity to grow smooth layers easily and to increase significantly variety of dielectrics other than SiO2.

Epi/epi/epi emitter has high efficiency, low divergence, stable uniform emission, long-lived performance.

Invention History

Published No

Announced No

Disclosed No

Next Three Months No

Described Yes - Results were written in "Flat Electron Emitters" by Thomas Novet and Alex Govyadinov [redacted]

Built Yes [redacted]

Government Contract No

Related Disclosure [redacted]

Innovation Workshop No

Witnesses

Witnesses Lori Tully Hewlett-Packard Company Corvallis [redacted]

James D Smith Hewlett-Packard Company Corvallis [redacted]

Classification

EXHIBIT A
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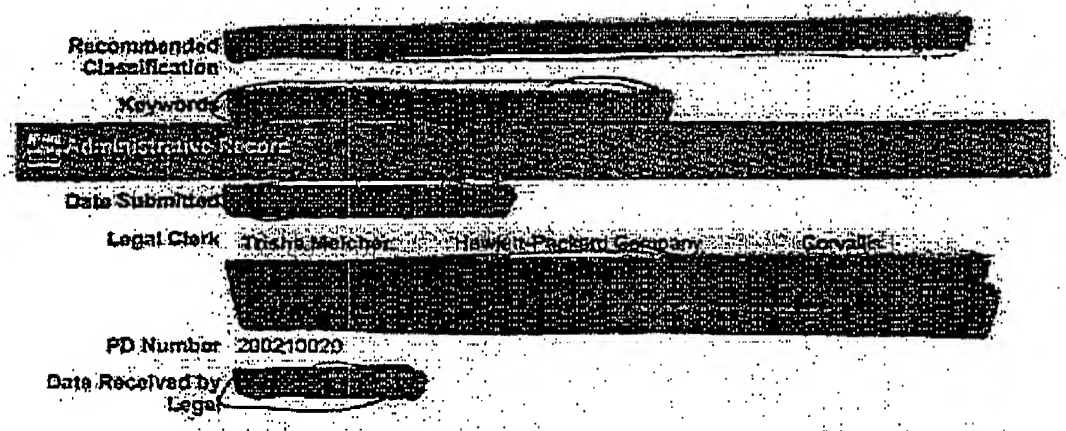

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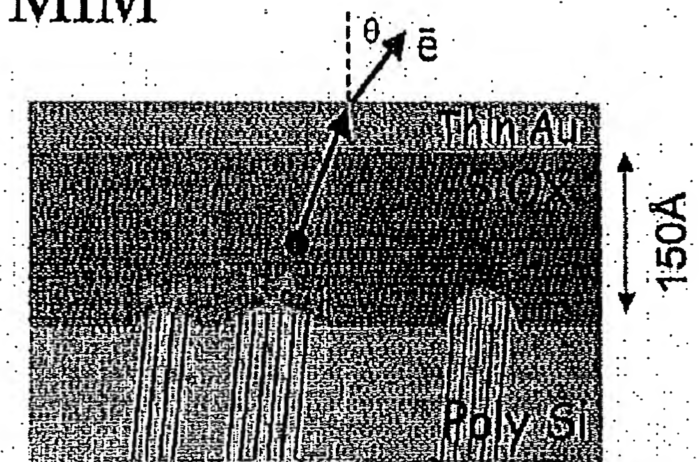
Prior solution: MIS with nonuniform field and flat MIM

Electric field curvature:

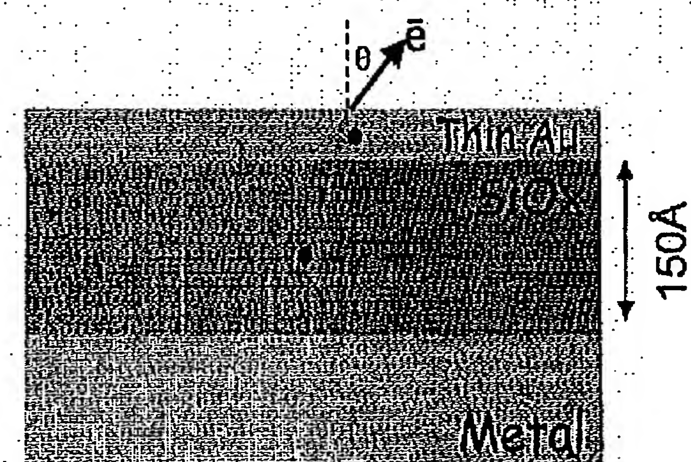
- Field strength will be greatest at sharp structures along the poly/oxide interface.
- The sharp structures will produce curvature in the electric field.
- Curved fields will produce diverging electron beams.

Electron scattering

- Electrons (ballistic mechanism) have scattering in the dielectric layer (particularly on defect sites), which introduce additional divergence
- Electrons have to go through thin metal to be released in vacuum. This induces more divergence



"Flat" MIS emitter



Flat MIM emitter

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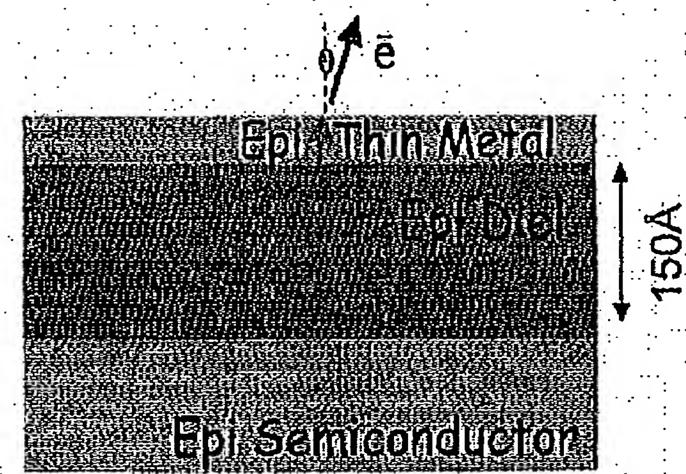
Proposed Epi-Epi-Epi emission structure

Advantages

- Less divergence because of flat field and no curved field.
- High resistive epi semiconductor plays role of ideal distributed ballast resistor and supplies uniform emission
- Minimized electron scattering using defectless dielectrics and thin top metal. Only electron refraction.



Epi-epi-epi emitter

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Proposed Emitter Process

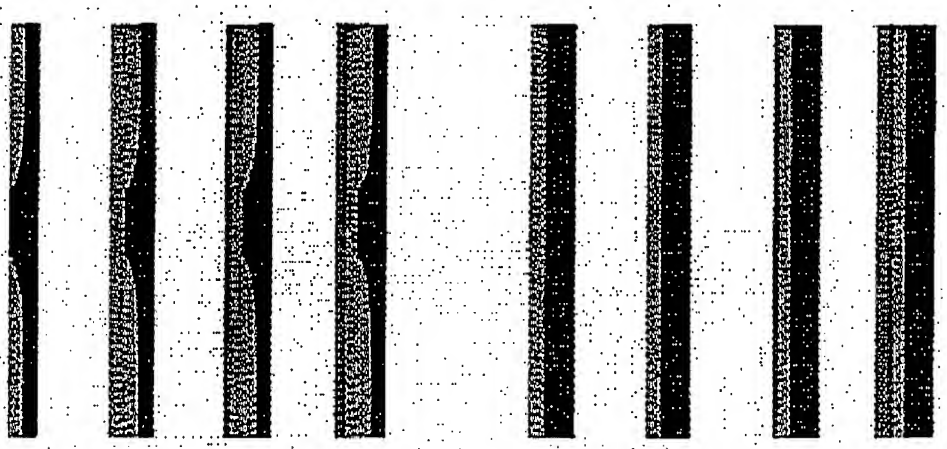

EXHIBIT A
PAGE 7 of 7

Tom Fitzsimons

From: MYERS,TIM (HP-Corvallis,ex1) [tim.myers@hp.com]
Sent: Wednesday, April 16, 2003 5:33 PM
To: 'Tom Fitzsimons'
Subject: RE: 200210020-1

Hi Tom, I received the application and will be reviewing it in short order. We will be filing the case and collecting signatures. I will get back to you soon. -Tim

-----Original Message-----
From: Tom Fitzsimons [mailto:tfitzsimons@gbclaw.net]
Sent: Wednesday, April 16, 2003 2:25 PM
To: TIM MYERS (HP-Corvallis,ex1) (E-mail)
Cc: sfallon@gbclaw.net
Subject: 200210020-1

Tim -

Attached is a draft application for your 200210020-1 (our 67292). The inventors have approved this draft.

Please let us know of any comments you have regarding the draft. Will we be filing this application or will we forward it to you for filing?

Yours truly,

Tom Fitzsimons
Greer, Burns & Crain, Ltd.
300 S. Wacker Dr., Suite 2500
Chicago, IL 60606-6501
(312)360-0080 Tel
(312)360-9315 Fax

EXHIBIT B

Tom Fitzsimons

From: Tom Fitzsimons [tfitzsimons@gbclaw.net]
Sent: Wednesday, May 07, 2003 3:36 PM
To: 'BENNING,PAUL (HP-Corvallis,ex1)'; 'NOVET,THOMAS (HP-Corvallis,ex1)'; 'paul_benning@hp.com'; 'alexander_govyadinov@hp.com'; 'robert_bicknell-tassius@hp.com'
Cc: 'sfallon@gbclaw.net'
Subject: RE: Epitaxial flat emitter

Tom, Paul, Alex, and Robert -

I heard back from the HP attorney regarding our draft patent application. He had a number of comments, with changes noted in the attached second draft. Most of the changes are typographical in nature, but some are not. Please review the changes at your early convenience.

[redacted]

Please contact me with any questions. Thanks for your continued help with this project.

Yours truly,

Tom Fitzsimons
Greer, Burns & Crain, Ltd.
300 S. Wacker Dr., Suite 2500
Chicago, IL 60606-6501
(312)360-0080 Tel
(312)360-9315 Fax

EXHIBIT C

Tom Fitzsimons

From: NOVET,THOMAS (HP-Corvallis,ex1) [thomas_novet@hp.com]
Sent: Wednesday, May 14, 2003 5:19 PM
To: 'Tom Fitzsimons'
Subject: RE: Patent Application

Tom,

I have talked with Bob and Alex; We have no disagreements with the latest draft.

-Tom Novet
Hewlett-Packard Company
(541)715-1356

-----Original Message-----
From: Tom Fitzsimons [mailto:tfitzsimons@gbclaw.net]
Sent: Wednesday, May 14, [illegible]
To: 'BENNING [illegible]
(HP-Cor[illegible] [illegible]om;
rober[illegible]
Sub[illegible]

EXHIBIT D

Tom Fitzsimons

From: Tom Fitzsimons [tfitzsimons@gbclaw.net]
Sent: Thursday, May 22, 2003 11:49 AM
To: 'MYERS,TIM (HP-Corvallis,ex1)'
Cc: 'sfallon@gbclaw.net'
Subject: HP 200210020-1


Tim -

Attached is a second draft of this application (Epitaxial layers). You will recall that you reviewed this a couple of weeks ago and that it had numerous typos. I have attended to these.

You also questioned whether the disclosed memory medium of InSe was the most current. I passed this question along to the inventors, and they are comfortable with disclosing InSe as an exemplary medium. No others appeared to be more preferred. The inventors have reviewed and approved of this second draft.

Please contact me after you have had a chance to look this over.

Yours truly,

Tom Fitzsimons
Greer, Burns & Crain, Ltd.
300 S. Wacker Dr., Suite 2500
Chicago, IL 60606-6501
(312)360-0080 Tel
(312)360-9315 Fax

EXHIBIT E

Tom Fitzsimons

From: MYERS,TIM (HP-Corvallis,ex1) [tim.myers@hp.com]
Sent: Tuesday, June 10, 2003 1:28 PM
To: 'Tom Fitzsimons'; TIM MYERS (HP-Corvallis,ex1) (E-mail)
Cc: sfallon@gbclaw.net
Subject: RE: HP 200210020-1

Hi Tom, I have reviewed the revised draft and have no further comments. Looks good. Please formalize and send to me for filing. We will collect the signatures. Thanks, Tim

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EXHIBIT F

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TELEPHONE (619) 234-1139

*ADMITTED IN CALIFORNIA AND ILLINOIS

June 20, 2003

VIA FEDERAL EXPRESS

Timothy F. Myers, Esq.
Hewlett-Packard Company
Legal Department - MS 422B
1000 NE Circle Boulevard
Corvallis, OR 97330-4239

Re: Novet et al. Patent Application
ELECTRON EMITTER WITH EPITAXIAL LAYERS
Your Ref No.: 200210020 – Our File No.: 3432.67292

Dear Tim:

As we discussed, enclosed for filing is a copy of the application and drawings, Transmittal, unexecuted Declaration and Assignment, foreign filing claims, an IDS that identifies references from the disclosure, and an electronic copy of the same, for the above-identified application. Please let us know if any corrections need to be made to any of the documents.

Yours truly,

GREER, BURNS & CRAIN, LTD.

By Thomas R. Fitzsimons

TRF:jls
Enclosures
cc: Steven P. Fallon, Esq.
K:\3432\67292\tmyers1.doc

EXHIBIT G